Supercapacitor-based Active Stabilization Method for DC Microgrid with Constant Power Load Causing Instantaneous Instability

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***Abstract*— In this paper, an active stabilization method using supercapacitor for a DC microgrid with a constant power load (CPL) causing instantaneous instability is proposed. DC microgrid has several advantages over its counterpart AC microgrid, such as high reliability, efficiency, and power quality with straightforward control. The share of tightly regulated loads, called CPL, is gradually increasing. These loads impose instantaneous instability problems in the DC bus as a major concern. As most of the transient components' frequencies are less than the switching frequency, and the magnitude is smaller than the DC link voltage, average model of the converters is sufficient to analyze the stability of the DC microgrid. Thus, in this paper, an average model is used. Lithium-Ion battery is used for energy time-shift to deal with the intermittent nature of renewables. A combined control strategy is developed for the battery and supercapacitor to facilitate active stabilization to reduce oscillation in DC bus voltage caused by CPL. Transient and high-frequency component of the reference current is assigned to the supercapacitor, whereas DC and low-frequency component reference current are assigned to the battery. Solar photovoltaic generation is considered, which interfaces to the DC bus via a practical DC-DC boost converter. This makes the stability analysis more generous. Simulation work is performed in MATLAB Simulink environment, and the results are verified with Hardware In Loop (HIL) OPAL-RT (RT-4510) simulator.**

Keywords—DC microgrid, supercapacitor, instantaneous instability, active stabilization, constant power loading.

I. INTRODUCTION

Gradual depletion of fossil fuel along with poor efficiency and rise in pollution has given rise to lesser inclination to fossil fuel [1]. Local power generation at the distribution voltage level is emerging to meet the demand for increasing per capita power consumption; this type of power generation is coined as distributed generation (DG) [2]. Distributed generation utilizes both conventional energy generation technologies like gas turbine as well as non-conventional renewable energy generators like solar panels, wind turbines, etc. The intermittent nature of renewable generation poses limitations. It requires an energy storage system to provide a time shift margin between energy production and consumption [3]. For example, when suffering from partial shedding, the SPV generator requires storage along a specific controller for normal operation.

A microgrid (MG) is defined as a conglomeration of DC and AC sources, localised storage, and local loads that functionalise in a controlled manner to enhance the reliability of the local power supply [4]. Microgrids can be classified as AC microgrid (ACMG) and DC microgrid (DCMG) and a hybrid of both [5]. SPV and FC generate DC power of low voltage rating and supply power to an AC utility grid through costly and inefficient power converters, even where the power may ultimately be delivered to a DC device [6]. Thus, DCMG is gaining more attention and popularity than its counterpart, ACMG. In addition, straightforward control, higher reliability, efficiency, and power quality, lack of need for frequency and reactive power control are merits of DCMG [7].

One of the major technical issues for DCMG is instantaneous instability occurring due to tightly regulated loads, which behave as a constant power load (CPL) [8].

In active stabilization schemes, advanced control strategies and software are employed to modify the impedances virtually on a real-time basis to confirm the stability of the DC/DC converters [9]. Reference [10] demonstrates improvement in stability depending on virtual impedance for DCMG with CPL. [11] reports Virtual Resistor Capacitor damper-based stabilization for CPL in DCMG. The concept of a 'Smart Resistor' is proposed based on an energy storage system to mitigate the instability [12]. The high-power density storage supercapacitor is utilized as an active stabilizer in DCMG [13].

Several passive and active stabilization techniques are reported in the literature to mitigate instability caused by CPL in DCMG. Few active stabilization-based storage systems are reported, but composite energy storage systems provides a new dynamic. This study adds no extra element, and the existing Composite Energy Storage System (CESS) infrastructure is assigned an additional function during instability/oscillation in DC bus voltage. Its normal function of time shift in energy and power balance is unchanged. The practical non-isolated boost DC-DC converter is considered to interface a practical DC source with the DC bus to make the design comprehensive and more suitable for renewables. The CESS supplies or absorbs power to suppress the DC bus oscillations. A combined controller for battery and supercapacitor controls their power sharing. The battery deals with average and low-power components, whereas the supercapacitor deals with transient and high-frequency components. A minute change in their respective SoC shows less stress on storage devices. MATLAB/Simulink results are studied for different conditions. OPAL-RT (OP4510) real-time simulator is used to validate the same.

The rest of the paper is organized as follows: Section 2 briefly explains the DC microgrid configuration and investigates its instability problem caused by CPL. Section 3 discusses a comprehensive small signal model of a DC-DC boost converter. The composite energy storage system, as an active stabilizer, is investigated in Section 4. Section 5 presents the MATLAB/Simulink and OPAL-RT results to demonstrate the developed control strategy. Finally, Section 6 summarizes this research work and concludes the paper.

II. DC MICROGRID CONFIGURATION AND STABILITY ANALYSIS WITH CONSTANT POWER LOAD

CPLs can produce transient instability in DCMGs that may create significant oscillations in their main bus voltages, which may even collapse. The DC microgrid configuration which is considered is shown in Figure 1. This DCMG consists of a practical DC source interfaced to a DC link via a practical DC-DC boost converter, a CESS, a CPL, and resistive loads.

A. Modeling of CPL

CPL and resistive load are connected at the DC bus at the voltage level of v_{dc}, whereas R_o and i_o are the resistance and current of resistive load, respectively. The tightly regulated converter, along with its output load, behaves as a CPL. The current-voltage characteristic of CPL is shown in Figure 2. Here, DC bus voltage, current, and power of CPL are represented by v_{dc}, i_{CPL}, and P_{CPL}, respectively. This current-voltage curve is a rectangular hyperbola governed by (1).

$$v_{dc} \times i_{CPL} = P_{CPL} = \text{Constant} \quad (1)$$

Due to the nonlinear relation between v_{dc} and i_{CPL} as given by (1), the entry of CPL in the DCMG configuration introduces nonlinearity. It can also be observed in Figure 2. By rearranging (1), (2) is obtained as:

$$i_{CPL} = \frac{P_{CPL}}{v_{dc}} \quad (2)$$

The incremental resistance can be mathematically expressed by (3) as a function of i_{CPL}. Partially differentiating both sides of (2) w.r.t. v_{dc},

$$\frac{\partial i_{CPL}}{\partial v_{dc}} = \frac{\partial}{\partial v_{dc}}\left(\frac{P_{CPL}}{v_{dc}}\right) = -\frac{P_{CPL}}{v_{dc}^2} = -\frac{i_{CPL}^2}{P_{CPL}} = -\frac{1}{R_{in}} \quad (3)$$

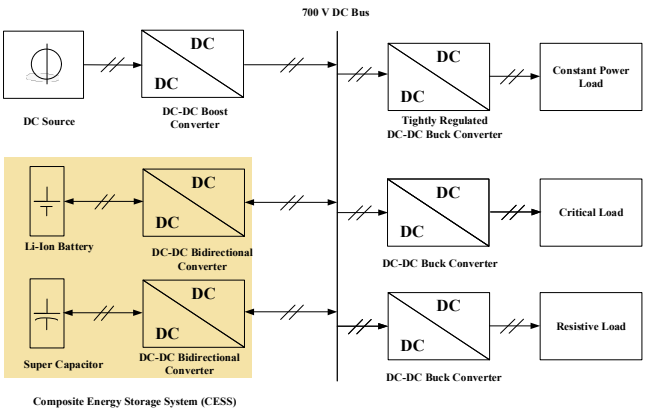


Fig. 1 Configuration of DCMG feeding CPL and resistive load with CESS

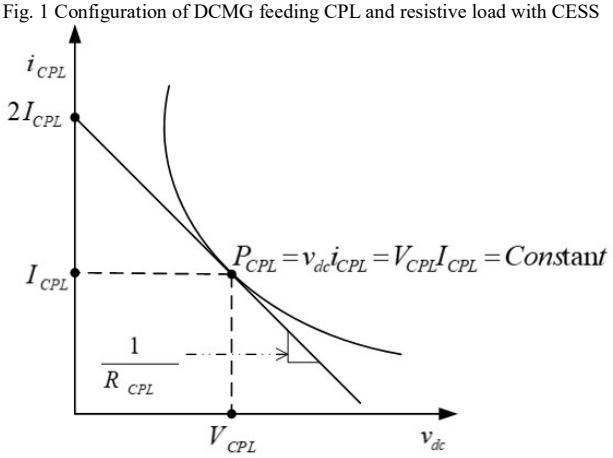


Fig. 2 Current-voltage characteristics of constant power load

Equations (1) – (3) advocate the nonlinear control schemes to address the instability problem caused by CPL In most cases, disturbance signal frequencies are much less than the converter switching frequency, and the magnitude is much smaller than the DC bus voltage. Thus, linearization can be implemented without losing accuracy for small signal disturbances around the operating point. In this paper, only approximated linearized model around the operating point (V_{dc}, I_{CPL}), is considered, which also satisfies equation (1). The current-voltage characteristic of CPL, as given in Figure 2, can be estimated by a straight line, *i.e.*, tangent to the power curve at the operational point, and (4) gives slope of the tangent.

At the operating point,

$$\left.\frac{\partial i_{CPL}}{\partial v_{dc}}\right|_{(V_{dc}, I_{CPL})} = -\left.\frac{P_{CPL}}{v_{dc}^2}\right|_{(V_{dc}, I_{CPL})} = -\frac{P_{CPL}}{V_{dc}^2} = -\frac{1}{R_{CPL}} \quad (4)$$

where R_{CPL} is the linear equivalent resistance of CPL that depends on the operating voltage and current.

The behavior of CPL is similar to that of a negative resistance (R_{CPL}) connected in conjunction with a current source $(2I_{CPL})$ depicted in Figure 3. Thus, around the operating point (V_{dc}, I_{CPL}), the relation for i_{CPL}, is given in (5).

$$i_{CPL} = 2I_{CPL} - \frac{v_{dc}}{R_{CPL}} \quad (5)$$

III. Modeling of Practical DC-DC Boost Converter

The DC-DC boost converter provides inherently destabilizing characteristics due to its right-half plane zero (RHP zero) in the s-plane, also called non-minimum phase zero [2]. Further, to make the model practical, parasitic parameters of all components are considered, as realized in Figure 3. Small signal analysis is used to investigate the stability issues and their mitigation. The DC-DC boost converter interfaces a practical voltage source (V_g) to the DC link (V_{dc}). The input voltage source parasitic resistance is denoted as r_g. The inductor (L) and capacitor (C) are the filter elements, and their DC resistance and Electrostatic resistances are r_L and r_C, respectively. The switch (S) has ON state resistance as r_{on}, and it is operated by duty ratio (d). The diode (D_i)has the forward voltage drop V_{fd} and resistance as r_d. R_0 is the resistance of load considered for this study. Inductor current (i_L) and capacitor voltage (v_c) are considered as state variables.

Practical DC-DC boost converter, with parasitic parameters, is analyzed for input-output voltage relationship, stable region of operation, and filter elements along with frequency domain analysis [3]. Accordingly, the input-output voltage relationship is modified and given by (6)

$$\frac{V_{dc}}{\left(V_g - D'V_{fd}\right)D'R_o(R_o + r_c)} = \frac{}{\left[\left(r_g + r_L + Dr_{on} + D'r_d\right)(R_o + r_c)\right] + \left[D'R_o(D'R_o + r_c)\right]} \quad (6)$$

where, $D' = 1 - D$ and D is the steady state duty ratio.

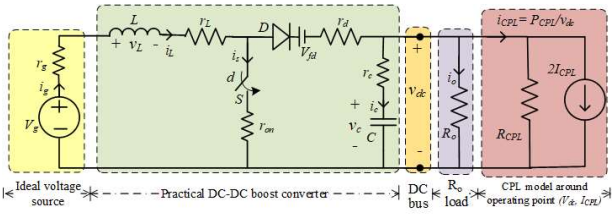


Fig. 3 Practical DC-DC boost converter interfaced with CPL and resistive load.

The solution of (6) for D'may have an imaginary part that leads the operation unstable. Thus, D is limited by D_{max}.

The DC-DC boost converter closed loop design requires small signal analysis-based transfer functions [4]. The plant transfer function for voltage control of a practical boost converter is as follows:

$$G_{vd}(s) = K\frac{\left(1 + \left(\frac{s}{\omega_z}\right)\right)\left(1 - \left(\frac{s}{\omega_{zrhp}}\right)\right)}{1 + \left(\frac{s}{\omega_p Q}\right) + \left(\frac{s}{\omega_p}\right)^2} \quad (7)$$

where K represents the gain, ω_z denotes the frequency of left-hand plane (LHP) zero, ω_{zrhp} represents the frequency of right-hand plane (RHP) zero, ω_p denotes the corner frequency for poles, and Q represents the quality factor.

IV. Modeling And Control of Composite Energy Storage System (CESS)

A composite energy storage system, combining both a high-energy-density battery pack and an enhanced-power density supercapacitor, meets both challenges of intermittent supply and storage requirement of high power density. Additionally, instability caused by CPL can also be addressed by CESS in the proposed suitable control strategies.

A. Model of Lithium-Ion Battery

The generic battery model with its parameters is depicted in Fig. 4.

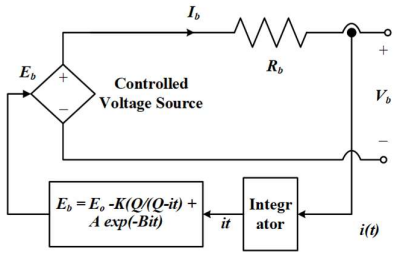


Fig. 4 Simplified nonlinear circuit model of battery.

Among different models for batteries involving various complexities, the most commonly used model includes parameters such as a controlled voltage source with an internal resistance connected in series with the voltage source [5]. The following equations govern the operation of the battery shown in Figure 4.

$$V_b = E_b - I_b R_b \quad (8)$$

$$E_b = E_o - K\frac{Q}{Q - \int i_b dt} + Aexp\left(B\int i_b dt\right) \quad (9)$$

$$SoC(t) = \frac{\int_0^t (i_b - E_b/R_b)\,dt}{Q} \quad (10)$$

In these equations; E_o, E_b, V_b, I_b, and R_b are the constant voltage, no load voltage, terminal voltage, battery current, and internal resistance of the battery, respectively. Whereas, battery maximum capacity (Q), state of charge (SoC), polarisation voltage (K), exponential voltage (A), and exponential battery capacity (B) are other important parameters.

B. Model of Supercapacitor

A supercapacitor is the outcome of the amalgamation of the chemical technology of a battery and the electrical technology of a capacitor. Unlike a battery, it is a power-density storage device. Capacitance as well as energy density of the supercapacitor is manifold times larger than that of electrolytic capacitors.

Several equivalent circuit models for supercapacitors are reported [7] and are shown in Figure 5. Energy stored (W_C) for ideal capacitor is given by (11),

$$W_C = \frac{1}{2}\ C_i V_o^2 \qquad (11)$$

where, C_i and V_o, are capacitance and terminal voltage, respectively.

Based on the RC ladder circuit as illustrated in Figure 5c, a three-branch equivalent circuit is considered [8] in this work for nonlinear analysis with v_1, v_2, and v_3 as voltage across C_1, C_2, and C_3, respectively, with experimental verification. The initial branch estimates its "fast" response, and the later branches depict the "intermediate" and "long" responses.

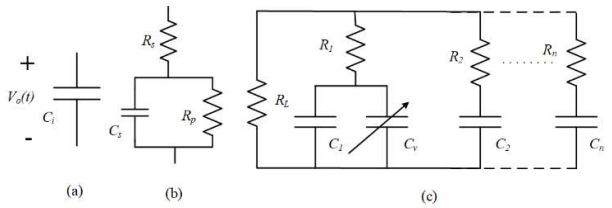


Fig. 5 Equivalent models of supercapacitor: (a) Capacitor under idealty (C_i), (b) Simplified model capacitance (C_s) comprising of a series resistor (R_s) and a parallel resistor (R_p), and (c) Resistor Capacitor ladder topology with its first branch having voltage-dependent capacitance (C_v) extendable to n branches.

C. Bidirectional DC-DC Converter for CESS interfacing

A DC-DC converter is utilized to facilitate the bidirectional power exchange amongst the CESS and the DC link, as per necessity. A typical bidirectional DC-DC converter (BDC) is depicted in Figure 6. It works as a buck converter in case of power flow from higher to lower voltage side and as a boost converter in vice-versa condition [9].

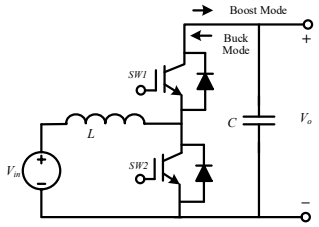


Fig. 6 BDC Topology

The transfer function for the inductor current-to-control and transfer function of inductor current to output voltage is obtained as (7):

$$G_{id}(s) = \frac{\Delta i_L(s)}{\Delta d(s)} = \frac{sCV_o + 2(1-D)I_L}{(LC)s^2 + \frac{L}{R}s + (1-D)^2} \qquad (12)$$

$$G_{iv}(s) = \frac{\Delta i_L(s)}{\Delta v_o(s)} = \frac{(1-D)V_o - (LI_L)s}{(CV_o)s + 2(1-D)I_L} \qquad (13)$$

The transfer functions described are used to design the closed loop controller [10].

D. Composite Control Scheme of Bidirectional Converters for Battery and Supercapacitor

Individual DC-DC converters are separately used to interface battery and supercapacitors to the DC link. The reference bus voltage when compared with the actual DC bus voltage generates the current reference with the outer Proportional-Integral (PI) controller. Low pass filter (LPF) as well as rate limiter (RTL) are utilized to segregate battery reference current (I_{bref}) and supercapacitor reference current (I_{scref}). The battery current error is also added with the transient component to take care of the battery uncompensated current. The transient reference produced is normalized using Battery voltage (V_b) and supercapacitor voltage (V_{sc}) as in Figure 7. The supercapacitor reference current (I_{scref}) estimated is fed to the inner supercapacitor current loop to remove oscillations on DC bus voltage along with transient control in DC bus voltage.

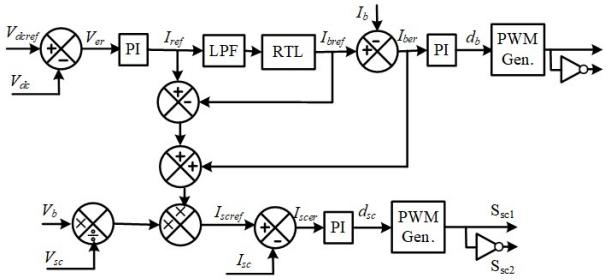


Fig. 7 Combined control for the proposed composite energy storage system.

V. Results And Discussion

The proposed strategy to improve the stability of DCMG supplying CPL with the help of CESS is first simulated in MATLAB/SIMULINK environment and then OPAL-RT real-time system is used to validate the same. The practical DC-DC boost converter's parameters are listed in Table.1, along with all parasitic values. The Bode frequency response plot of the control-to-output transfer function for ideal and practical DC-DC boost converters are depicted in Figure 8. The resonance peak is very small, and the phase crossover frequency is very large for the practical DC-DC boost converter compared to the ideal one. The practical boost converter and its controller are designed to feed a load of 10 kW.

TABLE I
PARAMETERS OF PRACTICAL DC-DC BOOST CONVERTER

Symbol	Quantity	Value
V_g	Input voltage	400 V
V_{dc}	DC bus voltage	700 V
r_g	Source resistance	0.05 Ω
L	Filter inductor	6.9 mH
r_L	Inductor parasitic resistance	0.06 Ω
C	Filter capacitor	15 mF
r_C	Capacitor parasitic resistance	0.1235 Ω
V_{fd}	Diode forward drop	0.8 V
r_d	Diode resistance	0.044 Ω
f	Switching frequency	10 kHz
R_o	Load resistance	49 Ω / 10kW

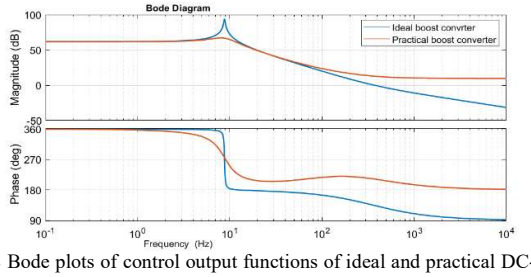


Fig. 8 Bode plots of control output functions of ideal and practical DC-DC

boost converter

A. MATLAB/SIMULINK Results

DC bus voltage for 20 kW CPL and 17.5 kW CPL without resistive load are presented in Figure 9a and b, respectively. The peak-to-peak magnitudes of oscillation are measured as 25 V and 16 V for 20 kW CPL and 17.5 kW CPL, respectively. Thus, the increment in CPL is very critical for stability.

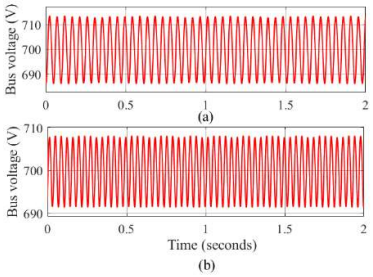


Fig.9 DC Bus voltage for CPL loads without resistive loads; a) 2kW CPL, and b) 17.5 kW CPL.

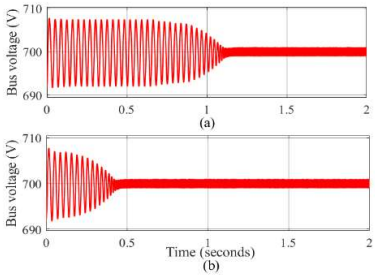


Fig.10 DC Bus voltages with a combination of CPL and resistive load; a) 9.5 kW CPL with 8 kW resistive load, and b) 8.75 kW CPL with 8.75 kW resistive load.

By introducing resistive load up to a certain value without changing the total load, DC voltage can be stabilized, as presented in Figure 10.

The DC link voltage stabilized in 1.05 and 0.4 seconds, with the resistive load at 8 kW and 8.75 kW, respectively. This investigation shows the relative effectiveness of resistive load to stabilize the DC bus voltage. In this paper, a CESS is mitigating the problem of instability caused by CPL. Two values of CPL are considered, one as continuous of 17.5 kW and another as pulse load of 10 kW for 0.8 seconds. DC bus voltage oscillations and corresponding CPL are presented in Figure 11. When CESS is applied, the DC bus voltage is stabilized. The extreme condition when CPL is 27.5 kW, the peak-to-peak magnitude of bus voltage oscillation is 68 V, as shown in Figure 13 for this, which is reduced by the CESS strategy to 4 V in Figure 12. Battery and supercapacitor currents are shown in Figure 12c and d. The battery handles a low-frequency component of controlling current, which is negligible in this case. Supercapacitor deals with high-frequency components of controlling current, which has inherent characteristics of high-power density devices. SoCs of the battery and supercapacitor are given in Figure13 during the stabilizing process. There is a minute change for both SoCs that again suggest minute stress.

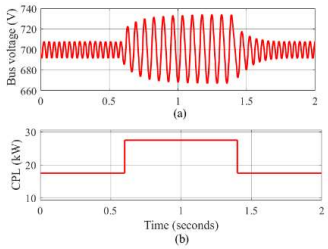


Fig.11 DCMG parameters without CES; a) DC bus voltage, and b) CPL

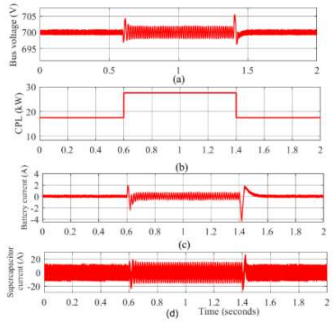


Fig.12 DCMG parameters with CESS; a) DC bus voltage, b) CPL, c) Battery current, and d) Supercapacitor current

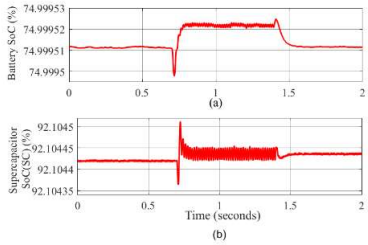


Fig. 13 SoCs of CESS; a) Battery SoC, and b) Supercapacitor

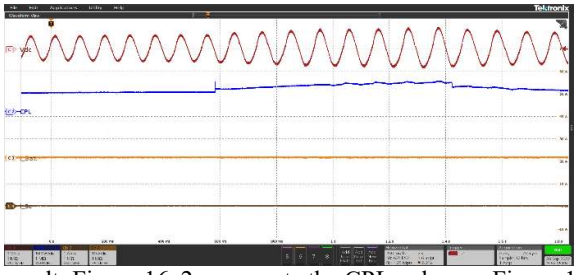
B. OPAL-RT Results

The OPAL-RT Real-Time simulator (Opal-RT 4510) is used for validation of the MATLAB/Simulink results, and the output waveforms are captured by a mixed signal oscilloscope (MSO58). The validation setup is shown in Figure 14.

Fig. 14 OPAL-RT Real-time Simulator.

The DC bus voltage is scaled down from 700V to 14 V to deal with RT- LAB simulator and Mixed Signal Oscilloscope. The CPL, battery current, and supercapacitor current are scaled to half at the RT simulator level. The CPL is scaled as 10 kW/ div, the battery current is scaled as 1A/div, and the capacitor current is scaled as 10A/div as depicted in Figure 15. Unmitigated DC bus voltage is shown in Figure 15c1 with oscillation and CPL in Figure15c2. The battery and supercapacitor are not connected; thus, their current remains zero, as seen in Figure15c3 and c4. A CPL of

17.5 kW is always connected to the DC bus. For time duration from 0.6 seconds to 1.4 seconds, an additional CPL of 10 kW as a pulse load is also applied, that further worsens the stability situation. DC bus voltage peak-to-peak oscillation is measured as 29 V and 60 V for 17.5 KW and 27.5 kW CPL, respectively, which illustrate the effect of the magnitude of CPL on stability and validates the MATLAB/Simulink result. Stabilized DC bus voltage with CESS is shown in Figure 16c1which shows that the peak-to-peak oscillation magnitude is less than 4 V which validates the simulation



result. Figure 16c2 represents the CPL, whereas Figure 16c3 and 16c4 shows battery and supercapacitor current currents, respectively. In the process of mitigation of instability, both battery and supercapacitor carry ripple current with zero average value. The battery is sensitive to this ripple current, but its peak-to-peak magnitude is less than 2 A which is not so severe, whereas, for the supercapacitor, it's 40 A and bearable.

Fig.15 DCMG parameters without CESS; **c1** DC Bus voltage, **c2** CPL, **c3** Battery Current, and **c4** Supercapacitor current.

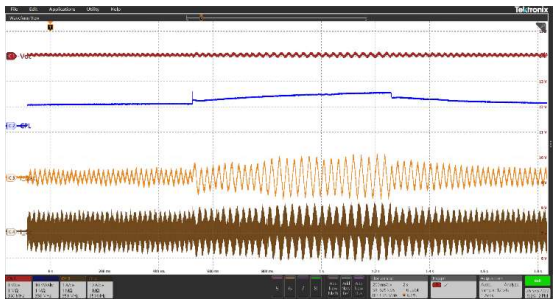


Fig.16. DCMG parameters with CESS; a) DC Bus voltage, b) CPL, c) Battery Current, and d) Supercapacitor current.

VI. Conclusion

A control strategy is investigated to mitigate the problem of instability due to constant power load in the DC microgrid. Existing infrastructure for the storage system consisting of battery and supercapacitor is utilized in this strategy. A practical boost converter with a robust controller can operate at 100% CPL and remain stable with a 50% additional CPL load of its rating. Both CPL and nonminimal-phase property of boost are addressed by the proper design of a practical DC-DC boost converter with closed loop controller design. 175% loading with CPL only shows oscillation in bus voltage as a peak-to-peak magnitude of 16 V, which is drastically increased further with the increment of CPL. With half share of the resistive load in this overloading (175%) condition, bus voltage stabilized. A similar result is obtained by load shedding. Both resistive loading and load shedding are not fully in the control of the power supplier/provider and are unsuitable. This proposed scheme mitigates the instability by monitoring the DC bus voltage, and at any instant surplus/deficit power is absorbed/supplied to maintain DC link voltage constant. The simulations are done for unstable conditions at 175% and 275% CPL. The CESS scheme makes DCMG stable without changing load pattern. The storage devices are also not suffering from specific stress, as seen by their SoCs. The MATLAB/Simulink results are verified with OPAL-RT real-time simulator.

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