

# DESIGN OF RECONFIGURABLE FREQUENCY SYNTHESIZER MEMRISTOR BASED HYBRID NCO FOR HARDWARE SECURITY APPLICATIONS

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**Abstract:** In System on Chips (SoCs), significant signals like cosine, sine, Linear Frequency Modulated (LFM), Gaussian, etc. are utilizing a numerically controlled oscillator (NCO) to produce on-chip. There are two methods for producing these signals: analogue circuitry or by digital circuitry. These signals are produced in a digital system using a numerically Controlled Oscillator (NCO), which converts them to analogue signals using a Digital to Analogue Converter (DAC). The crucial frequency translation required to extract the information from a digitally modulated signals are carried out by a Digital down Converter (DDC). The Numerically Controlled Oscillator (NCO), which is essential to the system's performance in digital down conversion, is the key element. Hence, in this design of reconfigurable frequency synthesizer memristor based hybrid NCO for hardware security applications is implemented. A wide range of frequencies are created by the NCO utilizing a fixed time period. By using a ROM (Read Only Memory) Look Up Table (LUT), it produces sine values. One of the primary issues is the size of the LUT as it must store sufficient sine samples to generate sine values at various frequencies. Therefore, the sine

output's bandwidth will be constrained by the size of the LUT. For the hybrid NCO, a development of state technique is recommended. Outputs are produced to show the sine and cosine values as we move through the states. To produce different frequency outputs, the state machine is timed with a changing clock signal. The remaining portion of the sinusoid may be produced by using the proper sign convention, and only a quarter of the sine/cosine function has to be saved.

**Key Words:** Digital to Analog Converter (DAC), Look Up Table (LUT), Digital Down Converter (DDC), Numerically Controlled Oscillator (NCO), memristor, Linear Frequency Modulated (LFM), System on Chips (SoCs), sine and cosine values, sign convention.

## **I. Introduction**

A precise reference signal whose frequency and phase can be accurately adjusted in real time is frequently required in communication and other circuits. This can be accomplished efficiently with the Numerically Controlled Oscillator (NCO) [1]. The temptation is to use only the MSB (Most Significant Bit) of the NCO output since the output reference signal for some applications is a square wave. However, it is excessive for the majority of communications operations [2]. This is profitable in low frequency applications like motor controllers. This is the output doesn't have an excessive level of jitter resulting from the zero crossings of this signal, which might vary by one period of the input clock between pulses [3].

An NCO block is a digital counter part of an analog oscillator circuit. There are two different NCO design options. A particular kind of NCO block uses specialized hardware,

such as the Coordinate Rotation Digital Computer (CORDIC) to calculate sinusoidal values [4]. Another kind of NCO block uses a Look up table (LUT) to store a sinusoidal signal with a fundamental frequency and then uses that signal to produce sinusoidal signals with different frequencies [5].

LUT based NCO blocks are very simple but have some disadvantages. Similar to, they are not capable of generating sinusoidal signals of any frequency [6]. But LUT based NCOs are hardware efficient than the other type of NCO block. Thus LUT based NCOs are mostly used because of their simplicity [7]. In this analysis, we will be focusing on designing an efficient LUT based NCO block to generate cosine or sinusoidal signals. The Field Programmable Gate Array (FPGA) Artix 7 is used to implement the LUT-based NCO block [8].

The principle of operation of a LUT based NCO is based on generating the cosine signal. The cosine signal with fundamental frequency ( $f_0$ ) can be stored in the LUT in three ways [9]. Either by storing the whole length of the signal, or storing half of the signal, or by storing only one fourth of the cosine signal [10]. This is possible due to symmetric and anti symmetric property of the cosine pulse. The third option is chosen to design the NCO and to reduce the memory storage elements from  $N$  to  $N/4+1$  [11].

Sinusoidal signals of different frequencies can be easily generated if the whole fundamental cosine signal is stored in LUT. But it is difficult to generate cosine signals if only  $N/4$  elements of the fundamental cosine signal are stored. The algorithm main intent is to generate cosine signals of different frequencies from the fundamental cosine signal. In

LUT,  $N/4+1$  elements of fundamental cosine signal is stored. The variable varies from 1 to  $N$  and 0 to  $N$ . The phase 180 signal is used to get 180 degree out of phase cosine signals [12].

Figure 1 displays the block diagram of the NCO. The major inputs to the block diagram are  $N$ , Phase, Start, Stop, *wav\_type* and phase 180 signals.  $N(=2^n)$  denotes the required period of the waveform, phase signal is used to apply required phase shift start pulse starts the NCO and a pulse at stop input can stop the NCO. Two types of signal generation are possible with this NCO, one is sine and another is cosine. The type of the signal is given at *wav\_type* input. If this signal is high then sine signal is output and if low then cosine signal is out. If instant 180 degree phase shift is required then it is possible by making the phase 180 signal high.

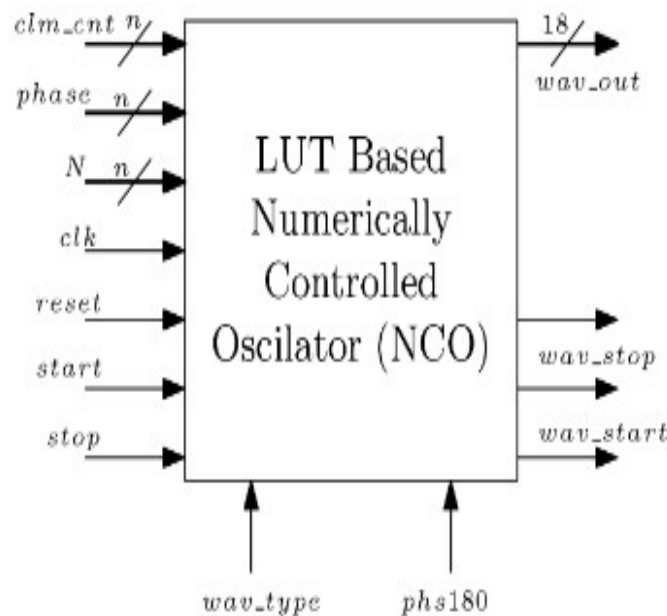


Fig. 1: The block diagram of the numerically controlled oscillator

Major outputs are wav\_out, wav\_stop and wav\_start. The wav\_start pulse indicates that the waveform is getting out of the NCO block. NCO gives output waveform through the wav\_out signal and it is of 18-bit width. The wav\_stop signal when delayed by two clock cycles indicates the end of a cycle. If only one cycle is required then wav\_stop signal can be connected to the stop input.

## 2. Conventional NCO

In software radio, a large portion of the signal processing is carried out in software on a platform with programmable hardware. To restore the original signal, the DDC applies frequency translation. The spectrum of the signal is shifted inside the DDC by combining the locally produced sinusoid with the digitized modulated input from the Analogue to Digital Converter (ADC). To find the region of the spectrum containing the desired signal, the mixed signal must be filtered. The filter normally have a narrow-band rejection of undesired lengths that is relatively high. If the input sample rate is used, this results in a costly filter. A different strategy is to use multiple rates, where the signal is initially decimated to a considerably lower sample rate using a less computationally demanding filter. A second, more complicated filter that operates at the decimated sample rate is used to clean up the signal after completion.

Figure (2) shows the typical NCO, also known as a local oscillator, producing sine and cosine signals using digital samples of two sine waves that are perfectly offset by 90 degrees in phase. It makes use of sine/cosine look-up tables and a digital phase accumulator (adder). The local oscillator receives input from the ADC clock. The ADC sample clock

frequency,  $f_s$ , is precisely matched by the sampling rate of the digital samples produced by the local oscillator. The complex mixer output samples at  $f_s$  since the data rates from the two mixer input sources are at the same ADC sampling rate,  $f_s$ .

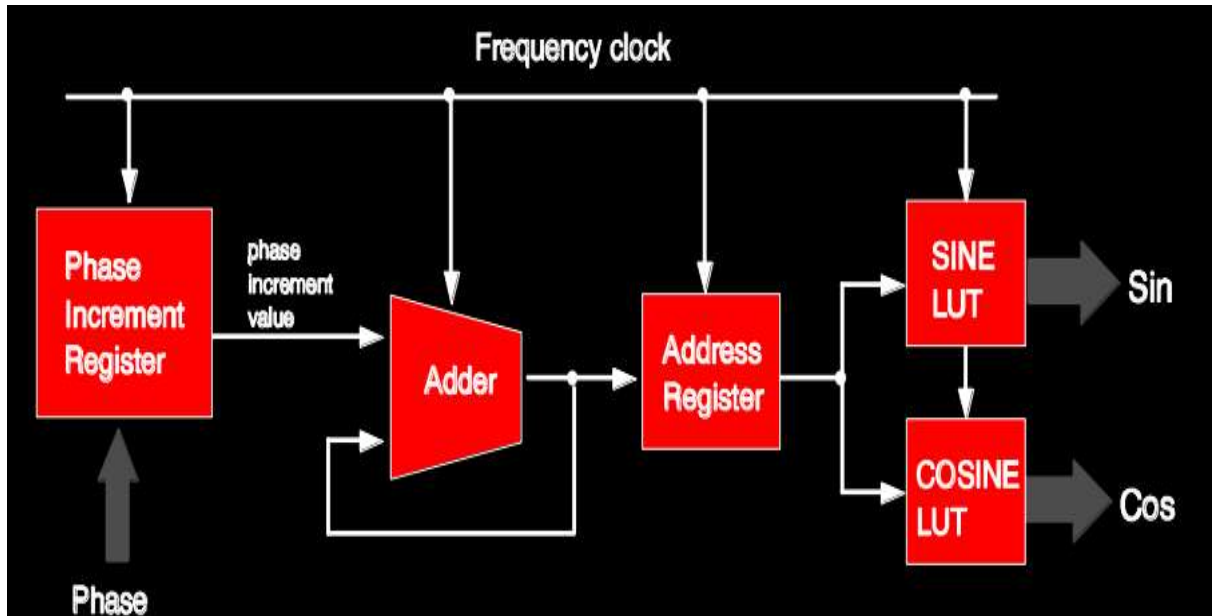


Fig. 2: Conventional NCO

The local oscillator's sine and cosine inputs result in in-phase and Quadrature (I and Q) outputs, which are crucial for preserving the phase information included in the input signal. At the full ADC sampling frequency,  $f_s$ , the decimating low pass filter receives input samples from the mixer output. It implements a FIR (Finite Impulse Response) filter transfer function using digital signal processing. The filter rejects all signals over a configurable cutoff frequency or bandwidth while passing all signals up to 0 Hz. The I and Q signals from the mixer are processed by the advanced digital filter.

The sine/cosine samples are stored in a ROM (Read Only Memory) LUT using the conventional NCO. Redundancy cannot be used in the system being developed since the

ROM (Read Only Memory) is fixed in nature. Additionally, random addressing is not required since the sine/cosine function follows a predetermined sequence. An address decoder, which is made up of multiplexers, manages the addressing in ROMs (Read Only Memory). The ROM (Read Only Memory) will surely contain  $n \times m$  memory cells that can store  $n$  words of length  $w$ .

### 3. Reconfigurable GDI Memristor Based Hybrid NCO

The below figure (3) shows the schematic of reconfigurable memristor based hybrid NCO. While designing this schematic 14 MOSFET's (Metal Oxide Semiconductor Field Effect Transistor's) are utilized. 1070 seconds total delay is obtained.

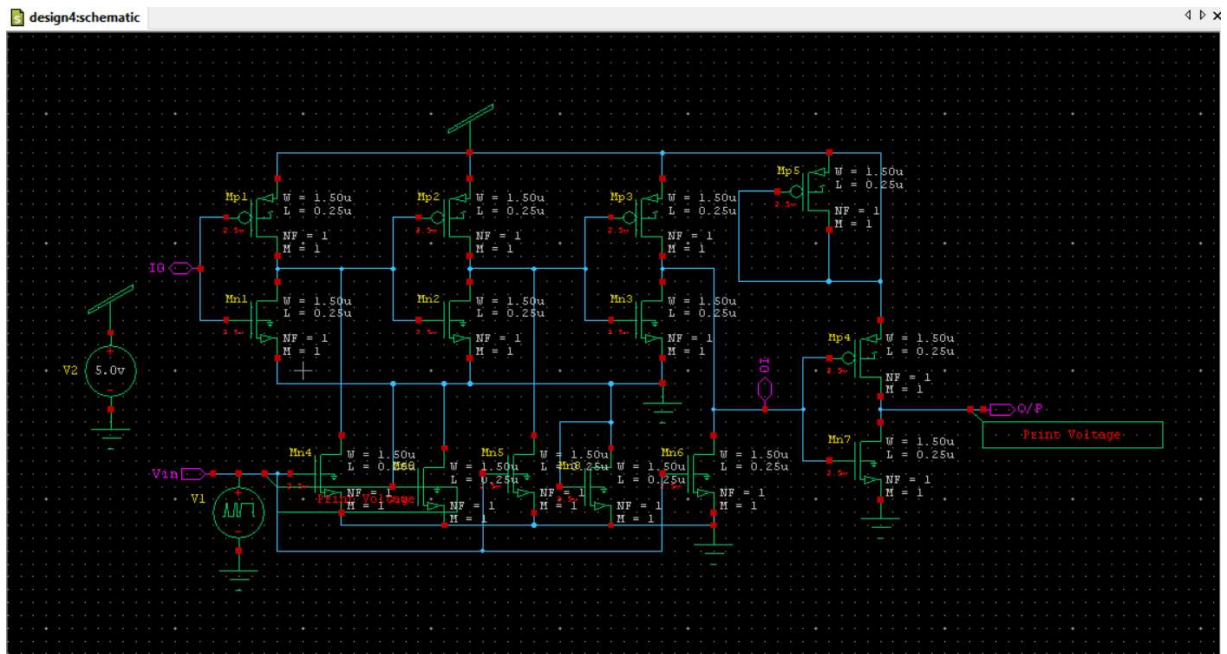


Fig. 3: Schematic of Reconfigurable GDI Memristor Based Hybrid NCO

Different clock waveforms are produced by the frequency synthesizer response to various frequency input words. Basically, it is made up of a binary counter and a frequency input register. To produce the sine in the second quadrant, the quad input inverts the sine in the

first quadrant along the y axis. The third and fourth quadrants are generated by reflecting the half-sine wave along the x axis (dc), allowing to the controlled inverters that are powered by the dc.

Angle resolution and sample rate are linked. The output speed will be slower but the angle resolution will be good with a high sampling rate. The tradeoffs between angular resolution and speed must be considered throughout design. By examining the required sine/cosine output at the slowest feasible movement, the required amount of samples each quarter may be determined.

The applied referenced clock frequency and the quantity of bits (N) used in the phase accumulator, determine the direct digital synthesizer's frequency resolution. The phase is determined by the NCO's continuous signals, which are produced at a certain Frequency Selected Word (FSW). This FSW establishes the signal frequency to be generated after being configured. The look-up table function receives appropriate binary words representing the currently selected phase from the phase accumulator output, which is continually produced.

The NCO block is efficient in terms of memory elements as it stores only one fourth part of the fundamental cosine signal. This NCO block has the capability to generate both sine or cosine signals. Signals can be phase shifted by any phase from 1 to N-1. This block is also capable of generating 180 degree out of phase signals without delaying. Besides generating sine or cosine signals of frequency difference  $f_0$ , this NCO block is also capable of generating signals with frequency difference  $f_m$  for  $N < 1024$ . The proposed design of NCO is scalable can be used in any complex digital system easily.



#### 4. Results & Discussion

The comparison table of conventional NCO and frequency synthesizer memristor based hybrid NCO is displayed in the table (1) below. In this total delay, total nodes and MOSFET's are provided. Compared with conventional NCO, frequency synthesizer memristor based hybrid NCO will reduce the usage of MOSFET's, nodes and total delay.

Table. 1: Comparison Table

S.No	Parameters	Conventional NCO	Frequency Synthesizer Memristor Based Hybrid NCO
1	Total Delay	2.83 seconds	1.70 seconds
2	Total Nodes	11	7
3	MOSFET's	16	14

The below figure (4) shows the comparison of total delay for conventional NCO and frequency synthesizer memristor based hybrid NCO. Frequency synthesizer memristor based hybrid NCO will reduce the total delay and memory usage compared with conventional NCO.

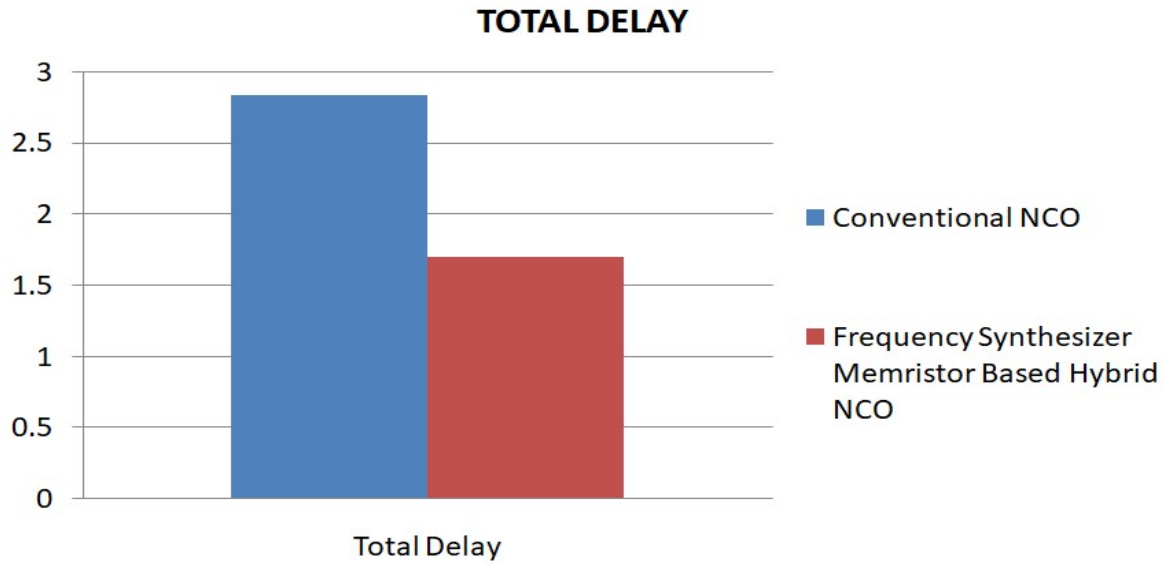


Fig. 4: Comparison of Total Delay for Conventional NCO and Frequency Synthesizer Memristor Based Hybrid NCO

The below figure (5) shows the comparison of total nodes for conventional NCO and frequency synthesizer memristor based hybrid NCO. Frequency synthesizer memristor based hybrid NCO will reduce the total nodes compared with conventional NCO.

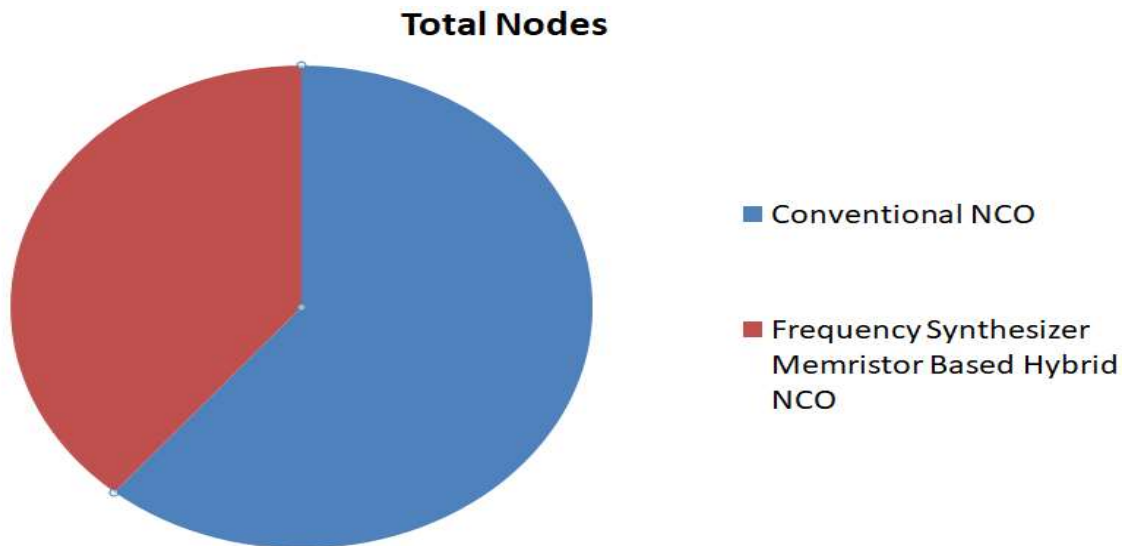


Fig. 5: Comparison of Total nodes for Conventional NCO and Frequency Synthesizer Memristor Based Hybrid NCO

The below figure (6) shows the comparison of number of MOSFET's for conventional NCO and frequency synthesizer memristor based hybrid NCO. Frequency synthesizer memristor based hybrid NCO will reduce the usage compared with conventional NCO.

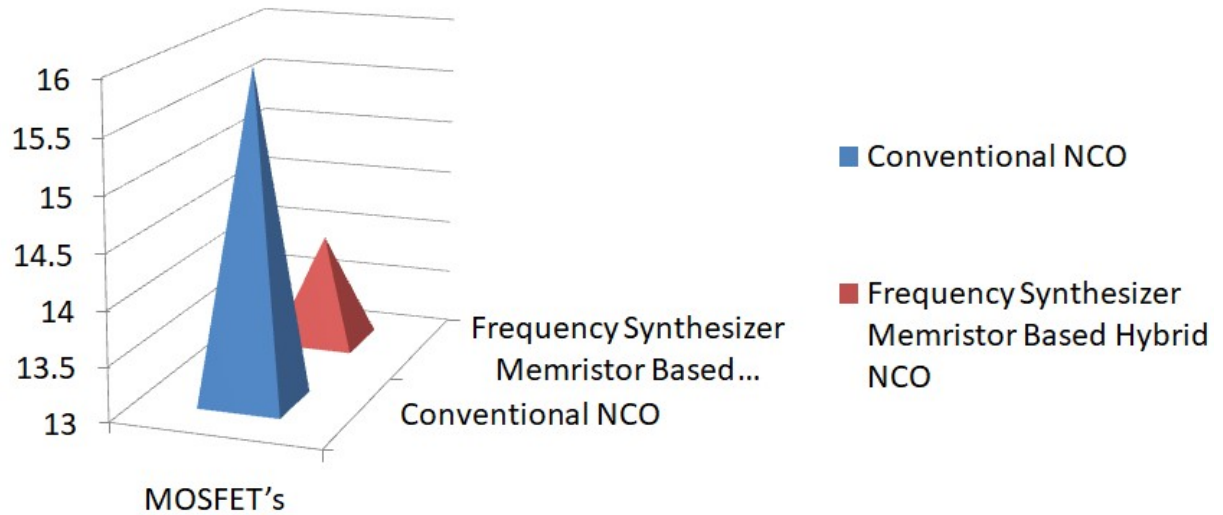


Fig. 6: Comparison of MOSFET's Conventional NCO and Frequency Synthesizer Memristor Based Hybrid NCO

The table (2) shows the Signal parameter of Frequency Synthesizer Memristor Based Hybrid NCO. This reference clock includes computed values for the frequency selected word, intended frequency, actual output frequency, frequency resolution, and signal to noise ratio characteristics.

Table 2: Signal Parameters Frequency Synthesizer Memristor Based Hybrid NCO

S.No	Parameter	Value
1	Reference Clock	2.55 GHz

2	Frequency Selective Word	06696B70
3	Desired Frequency	63.86 MHz
4	Actual Output Frequency	63.7755 MHz
5	Frequency Resolution	0.5937 Hz
6	Signal-to-Noise Ratio	188 dB

## 5. Conclusion

An oscillator whose design allows for the control of the waveform's phase or frequency is known as a numerically controlled oscillator. A linear frequency generator with configurable parameters is the numerically controlled oscillator. Hence in this paper, design of reconfigurable frequency synthesizer memristor based hybrid NCO for hardware security applications is implemented. Compared with conventional NCO, frequency synthesizer memristor based hybrid NCO will improve the accuracy and reduce the delay and memory usage. Therefore, in the future, the Numerically Controlled Oscillator (NCO) module functions as a timer that separates a frequency based on the increment values. The benefit of the addition approach over a simple counter-driven timer or a PWM (Pulse Width Modulation) is that it produces real linear frequency control as the divider set has no effect on the resolution of the division. The NCO is especially helpful for applications like lighting and ballast control, tone generators, and resonant power supplies that need linear frequency control, high frequency accuracy, and fine resolution at a given duty cycle.

## 6. References

- [1] Monika kushwaha, U. M Gokhale, “Design and Simulation of Direct Digital Synthesizer for Wireless Applications” , Journal of The International Association of Advanced Technology and Science, Vol. 16 March 2015
- [2] Priyankap. Chopda, Kavita S. Tated&Jayant J. Chopade, “Sine Wave Generation Using Numerically Controlled Oscillator Module”, BEST: International Journal of Management, Information Technology and Engineering (BEST: IJMITE) ISSN(P): 2348-0513;ISSN(E): 2454- 471X Vol. 3, Issue 7, Jul 2015, 35-40.
- [3] IreneuszJaniszewski, Bernhard Hoppe, Associate Member, IEEE, and Hermann Meuth, “Numerically Controlled Oscillators with Hybrid Function Generators”, IEEE transactions on ultrasonics, ferroelectrics, and frequency control, vol. 49, 2015 no. 7, july.
- [4] Gaurav Gupta, Monika Kapoor, “An Improved Analog Waveforms Generation Technique using Direct Digital Synthesizer”, International Journal of Computer Applications (0975 – 8887) Volume 78 – No.5, September 2014.
- [5] R. Ertl and J. Baier, “Increasing the Frequency Resolution of NCO-Systems Using a Circuit Based on a Digital Adder,” IEEE Trans. Circuits Systems II: Analog and Digital Signal Processing, vol. 43, Mar. 2013, pp. 266-269.
- [6] Mehmet Sonmez and Ayhan Akbal “FPGA-Based BASK and BPSK Modulators Using VHDL: Design, Applications and Performance Comparison for Different Modulator Algorithms” In March 2012, International Journal of Computer Applications (0975 – 8887) Volume 42– No.13, March 2012.
- [7] Manoj Kollam, S.A.S.KrishnaChaithanya, Nagarajukommu, “Design and Implementation of An Enhanced Dds Based Digital Modulator for Multiple Modulation Schemes”,

International Journal of Smart Sensors and Ad Hoc Networks (IJSSAN) Volume-1, Issue-1, 2011.

[8] Miller, Brian M., "Numerically controlled oscillator and method of operation", issued October 14, 2011.

[9] F. Gonzalez-Espin, G. Garcera, I. Patrao, and E. Figueres, "An adaptive control system for three-phase photovoltaic inverters working in a polluted and variable frequency electric grid," IEEE Trans. Power Electron., vol. 27, no. 10, pp. 4248-4261, Oct 2011.

[10] S. Golestan, M. Monfared, F. D. Freijedo, J. M. Guerrero, "Design and tuning of a modified power based PLL for single-phase grid connected power conditioning systems," IEEE Trans. Power Electron., vol. 27, no.8, pp. 3639-3650, Aug. 2010.

[11] Y. F. Wang, and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," IEEE Trans. Power Electron., vol. 26, no. 7, pp. 1987-1997, Jul. 2010.

[12] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-locked loop for series-connected converters," IEEE Trans. Power Del., vol. 20, no. 1, pp. 300-308, Jan. 2009.