Surge Voltage Suppression Using Power Device Embedded Module for Half-bridge DC-DC Converter

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***Abstract*—This paper clarified the half-bridge dc-dc converter's surge voltage generation mechanism and validated the performance of a half-bridge power device embedded module (HB-PDEM) for surge voltage suppression. Simulation and experimental results demonstrate that the proposed half-bridge power module achieved an extremely low parasitic inductance and effectively suppressed the surge voltage.**

Keywords— Half-bridge power device embedded module (HB-PDEM); TO-247 package; parasitic inductance; surge voltage; half-bridge dc-dc converter.

I. INTRODUCTION

In smart grid applications, a typical power supply consists of two components: the PFC converter and the DC-DC converter. To attain a high power factor and minimize the total harmonic distortion (THD) of the input current, the utilization of a PFC converter is necessary [1]-[8]. The half-bridge dc-dc converter is a popular choice for the dc-dc converter in smart grid applications due to its simplicity and easy controllability [1], [2]. In order to increase efficiency, the input voltage of the half-bridge dc-dc converter is raised to a higher level. As a result, the converter utilizes the half-bridge power module (HB-PM) for its main switches instead of the discrete MOSFETs to accommodate the higher input voltage. Fig. 1 shows the topology of the half-bridge dc-dc converter utilizing the HB-PM.

During the switching transition, the resonance between the parasitic inductance and the parasitic capacitances leads to a high surge voltage [1], [2]. The surge voltage adversely affects both efficiency and EMI. An effective method for suppressing the high surge voltage involves utilizing a snubber circuit, which may result in increased power loss and a larger circuit size. Another effective approach is to decrease the parasitic inductance of HB-PM [1].

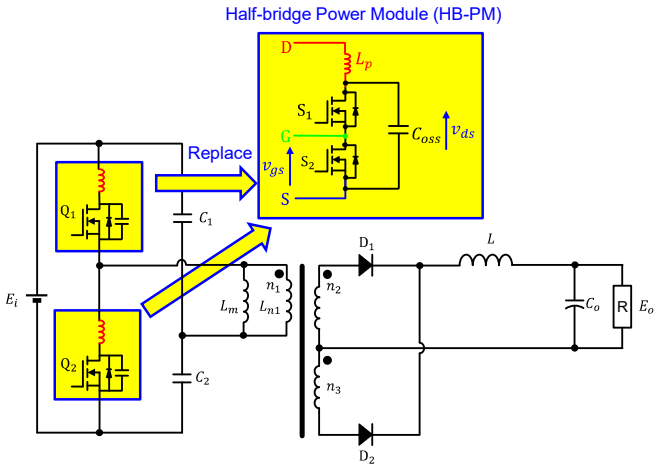
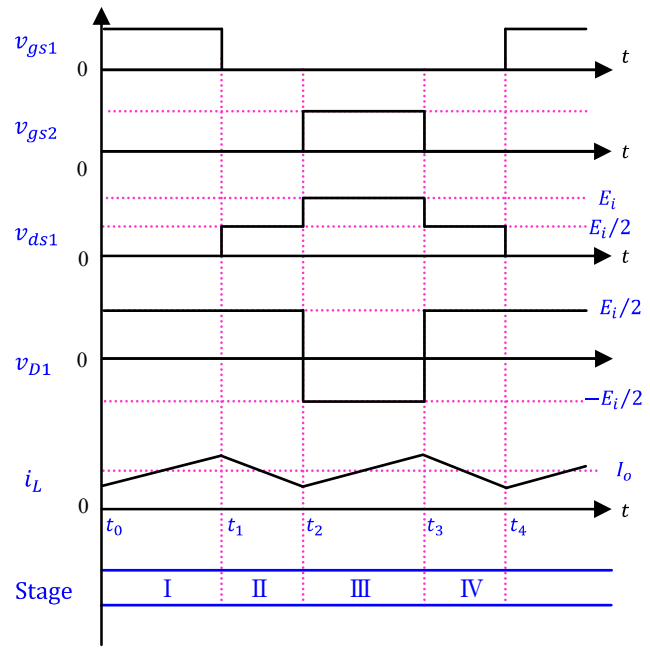


Fig. 1. Half-bridge dc-dc converter utilizing half-bridge power module (HB-PM).

Dy the development of HB-PM, several HB-PMs with low parasitic inductance have been presented [9]-[17]. A half-bridge power device embedded module (HB-PDEM) is proposed in [1]. The proposed HB-PDEM combines two chips in one package and has an extremely low parasitic inductance of 1.6 nH at 60 kHz. The parasitic inductance of the HB-PDEM is approximately one-twentieth of the conventional TO-247 packaged HB-PM. Nonetheless, the performance of the proposed HB-PDEM for surge voltage suppression has not been validated enough.

This paper aims to clarify the half-bridge dc-dc converter's surge voltage generation mechanism and to confirm the effectiveness of the proposed HB-PDEM in suppressing surge voltage. The surge voltage generation mechanism is described in section II. Section III presented the simulated parasitic inductances of the conventional TO-247 packaged HB-PM



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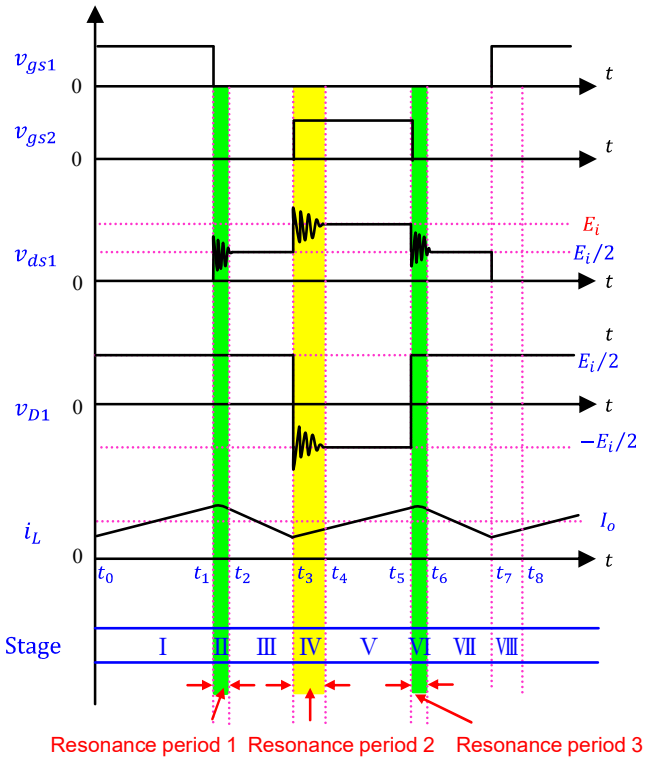
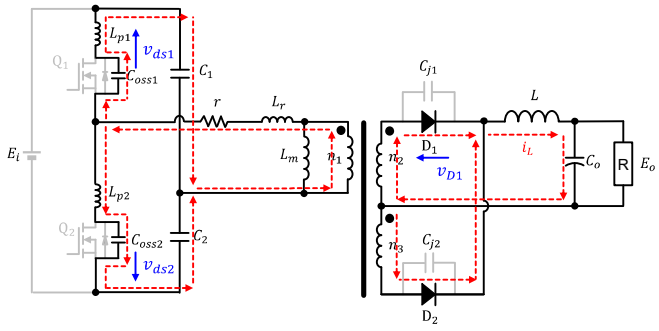


(b)

Fig. 2. Key waveforms of the half-bridge dc-dc converter. (a) Ideally case. (b) Case of considering the effects of parasitic inductances and parasitic capacitances.

and the proposed HB-PDEM. The simulation and experimental results in Section IV demonstrate the effectiveness of surge voltage suppression in the proposed HB-PDEM. Finally, conclusions are drawn in Section V.



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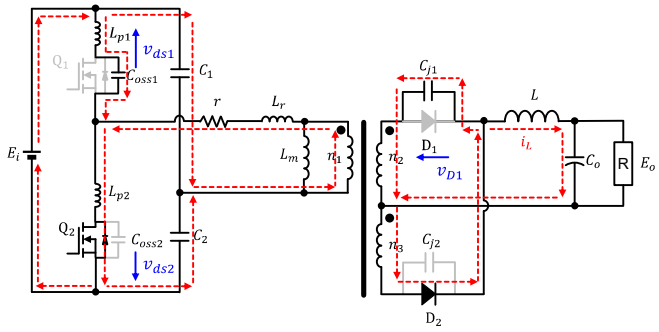

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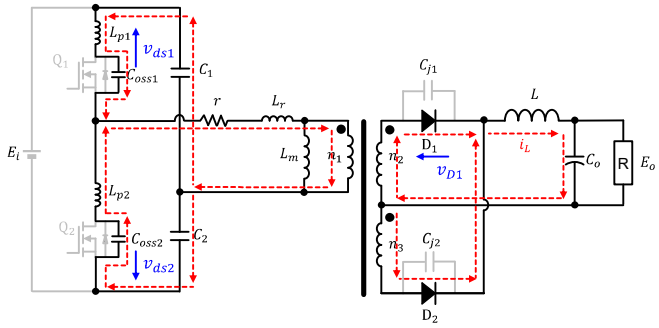


(c)

Fig. 3. Equivalent circuits of the half-bridge dc-dc converter's resonance periods. (a) Resonance period 1 (stage II). (b) Resonance period 2 (stage IV). (c) Resonance period 3 (stage VI).

II. Surge Voltage Generation Mechanism

This section clarifies the half-bridge dc-dc converter's surge voltage generation mechanism. Fig. 2 shows the half-bridge dc-dc converter's key waveforms when considering the parasitic parameters' effects. Fig. 3 gives the equivalent circuits of the surge resonance periods (stage II, stage IV, stage VI). In Fig. 3, C_{oss1} and C_{oss2} indicate the parasitic capacitances of switches Q_1 and Q_2, respectively. The parasitic inductances of switches Q_1 and Q_2 are represented by L_{p1} and L_{p2}, respectively. The voltages across the drain and source of Q_1 and Q_2 are respectively represented by v_{ds1}

and v_{ds2}. L_r indicates the parasitic inductance of the transformer's primary side, and r is the parasitic resistance. C_{j1} and C_{j2} indicate the parasitic capacitances of secondary side diodes D_1 and D_2, respectively. v_{D1} indicates the voltage across the diode.

Stage II ($t_1 \sim t_2$): As shown in Fig. 3(a), the parasitic inductances ($L_r + L_{p1}$ or L_{p2}) resonate with the parasitic capacitances C_{oss1} and C_{oss2} during this stage. Due to this resonance period, high surge voltages in v_{ds1} and v_{ds2} occur. On the secondary side, since D_1 and D_2 are turned on in this stage, and no current flows to C_{j1} and C_{j2}; thus, there is no surge voltage occurring in D_1 and D_2.

Stage IV ($t_3 \sim t_4$): On the primary side, the parasitic inductance L_{p1} resonates with the parasitic capacitance C_{oss1}, resulting in a significant surge of v_{ds1}. Q_2 is not experiencing any surge as it is currently turned on. On the secondary side, D_2 is turned on, and D_1 is turned off. L resonates with the parasitic capacitance C_{j1} and leads to a high surge in v_{D1}.

Stage VI ($t_5 \sim t_6$): In this stage, the equivalent circuit remains the same as in stage II, but the direction of the current flow is reversed. The same surge voltage as stage II is experienced in this stage.

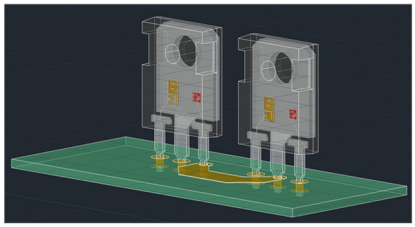
III. Simulated Parasitic Inductances in Conventional HB-PM and Proposed HB-PDEM

Fig. 4 shows the simulation models of the conventional TO-247 packaged HB-PM and the proposed HB-PDEM, respectively. As shown in Fig. 4(a), the conventional HB-PM utilizes the lead frame package (TO-247 package), which is mounted on two PCBs. The wiring inside the lead frame package is connected by thin aluminum wires with a diameter of approximately 300 µm, which leads to a large parasitic inductance. Compared to the TO-247 packaged HB-PM, the proposed HB-PDEM has the advantage of incorporating two chips in a single package, as depicted in Fig. 4(b), thereby reducing the parasitic inductance to a great extent.

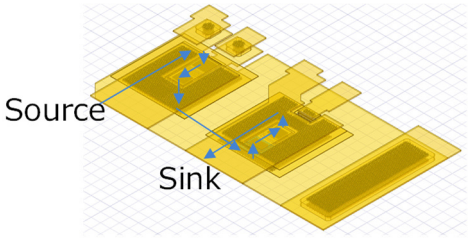
The parasitic inductances L_p in the conventional TO-247 packaged HB-PM and the proposed HB-PDEM are simulated by the soft Ansys Q3D Extractor. The simulation results are shown in Fig. 5. It can be found that L_p in the conventional TO-247 packaged HB-PM is simulated as 35 nH at 60kHz, and it is only 1.6 nH in the proposed HB-PDEM. The results show that the proposed HB-PDEM can effectively decrease L_p.

IV. Simulation and Experimental Verification

To confirm the effectiveness of the proposed HB-PDEM in suppressing surge voltage, the surge of v_{ds} in the discrete MOSFET and the proposed HB-PDEM is tested by simulation and experiments. The simulation verification is conducted with the parameters temporarily set as follows: input voltage/output voltage of 375 V/24 V, output power of 288 W, and switching frequency of 60 kHz. For comparison with the HB-PDEM, a discrete MOSFET packaged in TO-247


Simulation model of conventional TO-247 packaged HB-PM.

(a)



(b)

Fig. 4. Simulation models. (a) Conventional TO-247 packaged HB-PM. (b) Proposed HB-PDEM.

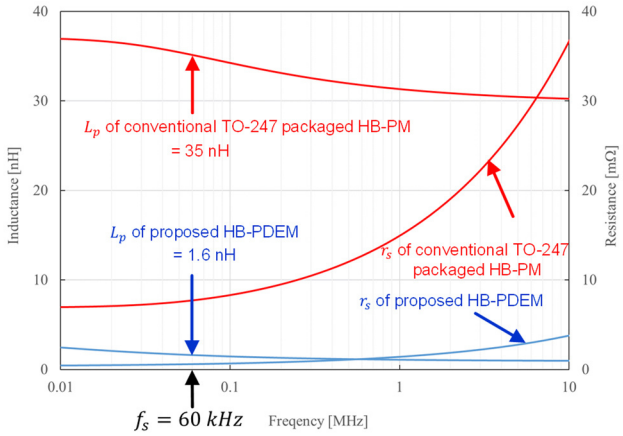
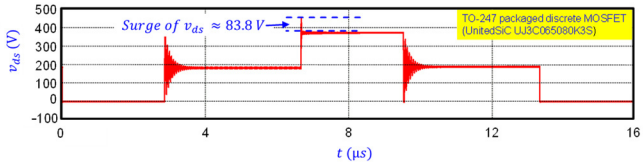


Fig. 5. Simulated parasitic inductances in the conventional TO-247 packaged HB-PM and the proposed HB-PDEM.



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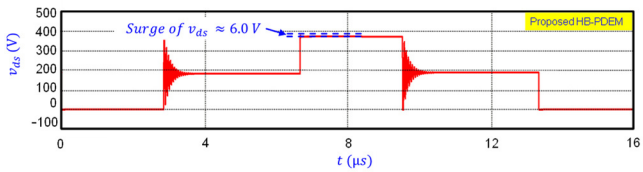

(b)

Fig. 6. Simulated surge of drain-to-source voltage comparison. (a) TO-247 packaged discrete MOSFET (UnitedSiC UJ3C065080K3S). (b) Proposed HB-PDEM.

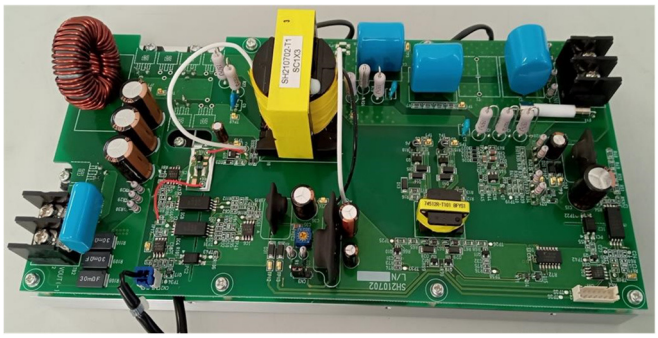

Fig. 7. 288 W prototype of the half-bridge dc-dc converter.

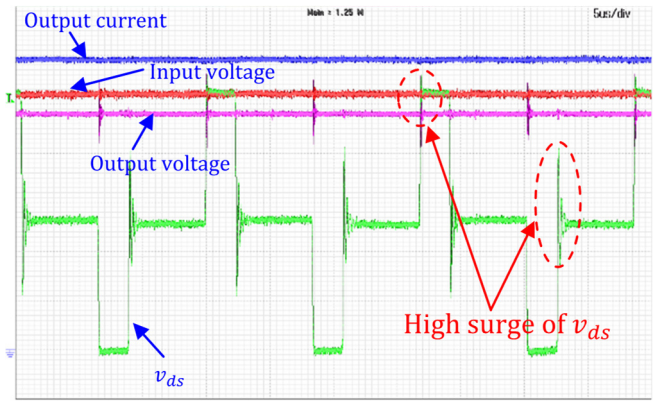

Fig. 8. Experimental switching waveforms of the half-bridge dc-dc converter using the discrete MOSFET.

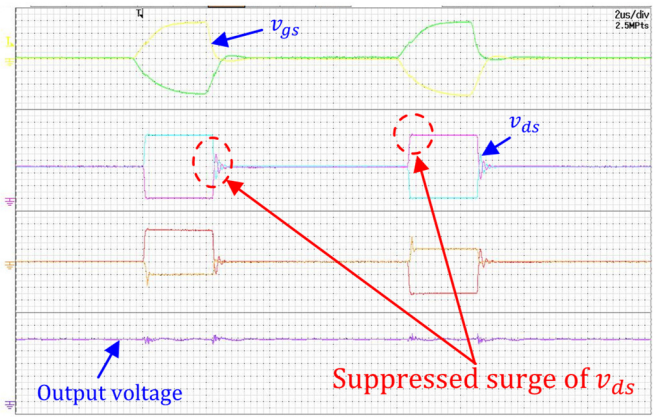

Fig. 9. Experimental switching waveforms of the half-bridge dc-dc converter using the proposed HB-PDEM.

(UnitedSiC UJ3C065080K3S) has been chosen. Based on the UnitedSiC UJ3C065080K3S datasheet [18], the parasitic capacitance C_{oss} is calculated as 61 pF. According to Fig. 5, the parasitic inductance L_p is estimated to be 17 nH. Fig. 6 shows the surge of v_{ds} comparison between the discrete MOSFET and the proposed HB-PDEM. It is shown that the surge of v_{ds} is suppressed from 83.8 V to 6.0 V owing to the extremely low L_p (1.6 nH at 60 kHz) in the proposed HB-PDEM.

Then, the surge of v_{ds} is tested in a 288 W experiment prototype of the half-bridge dc-dc converter. The rated input/output voltages are 500V/24V. The switching frequency is 60 kHz. The prototype photo is shown in Fig. 7.

Fig. 8 shows the waveform of v_{ds} using the TO-247 packaged discrete MOSFET. It can be found that a high surge of v_{ds} is measured in the discrete MOSFET due to the resonance between the large parasitic inductance and parasitic capacitance.

Fig. 9 shows the waveforms of v_{ds} using the proposed HB-PDEM. Owing to an extremely low L_p (1.6 nH at 60 kHz) achieved in the proposed HB-PDEM; therefore, it is observed that the surge of v_{ds} is very low. The experimental comparison verifies that the proposed HB-PDEM with extremely low L_p can significantly suppress the surge of v_{ds}.

V. Conclusion

The performance of a half-bridge power device embedded module with low parasitic inductance is validated in this paper. The half-bridge dc-dc converter's surge voltage generation mechanism is clarified. The parasitic inductance in the proposed HB-PDEM is 1.6 nH at 60 kHz, much lower than in the conventional TO-247 packaged HB-PM (35 nH at 60 kHz). Experimental switching waveforms verified that the proposed HB-PDEM effectively suppressed surge voltage.

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