Design and Implementation of 125 and 243 Level Cascaded H-Bridge Multilevel Inverter using Binary Search Algorithm

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***Abstract*—Since the evolvement of multilevel inverters in power conversion systems, achieving a larger number of output voltage levels using the least number of switches has been the topic of research for many researchers. This paper presents two unique asymmetrical configurations of Cascaded H-Bridge Multilevel Inverter (CHB-MLI) to obtain 125 ad 243 levels using five H-bridges. For the implementation of proposed configurations, the binary search algorithm is used through Synchronous Transport Module for designing PulseWidth Modulation (PWM). MATLAB is used for simulation using the designed PWM technique while it is implemented on hardware through STM32F407 using Keil uVision, STM CubeMX, and STM Studio. Voltage waveform with lesser Total Harmonic Distortion (THD) than conventional H-bridge is achieved.**

I. Introduction

The energy obtained from renewable energy sources can't be used directly without using DC-DC converters or DC-AC inverters. To make it feasible for injecting into the grid, voltage, current, frequency, phase angle, and phase difference of the waveform of the inverter should be same as that of the grid [1]-[2]. Multilevel Inverter (MLI) is a power electronic device that generates staircase output voltage waveform using multiple DC voltages at the input [3]. MLI produces a smoother waveform with lesser THD. The output voltage waveform of MLI has lower dv/dt which enhances its applications [4]-[5]. That's why MLIs are mostly used in power electronics, renewable energy, and HVDC transmission lines [6]- [7].

There are a number of topologies of MLIs to generate staircase output voltage waveform. Few of them are Diode Clamped MLI (DC-MLI) also known as Neutral Point Clamped MLI (NPC-MLI) [8], Cascaded H-Bridge MLI (CHB-MLI) and Flying Capacitor MLI (FC-MLI) [9]. NPC-MLI uses diodes [8] while FC-MLI uses capacitors [9] to provide limited voltage to the switches. Capacitor voltage can't be maintained according to the desired values in NPC-MLI which causes unbalance across the switches. In FC-MLI, redundant switching is required to balance the flying capacitors which causes switching losses. Since the input voltage is divided across the capacitors, so the output voltage cannot exceed half of the input voltage in NPC-MLI as well as FC-MLI. NPC-MLI and FC-MLI are good for three-level inverters but for higher levels, the number of electronic devices increases, and the circuit becomes unsymmetrical. CHB-MLI doesn't need any clamping capacitor or capacitors across the supply [10]-[11]. CHB-MLI also uses separate DC sources for each H-bridge hence according to the required DC voltage rating, it can easily be integrated with renewable energy resources [12]. The structure of CHB-MLI is very symmetrical as we increase the number of levels which makes its implementation much easier. Hence, we can say that out of these three topologies, CHB-MLI is the most suitable one for industrial applications. As far as CHB-MLI is concerned, the only issue in CHB-MLI is the larger number of switches for higher levels. Conventional full-wave H-Bridge uses four switches and as a result, generates three voltage levels $(+V_{dc}, 0, -V_{dc})$. Conventional or symmetrical CHB-MLI follows 2N+1 relation for enhancing the number of levels (N represents the number of H-bridges). Researchers have modified the H-bridge configuration and tried to enhance the number of levels using asymmetric DC voltage levels [13]. In [14], five-level output voltage is generated using seven switches. Different schemes have been introduced in [15] where six switches and three DC link voltages generate output voltage containing seven-levels. In [16], various cases have been discussed that produces 13, 15, 19, and 27 level output voltage using twelve switches. The ratio of asymmetric DC voltage levels is unique and different from 1:1:1… . Asymmetric DC voltages are capable of generating larger levels and a waveform with lesser THD

using lesser switches, DC supplies and gate drivers [17].
The proposed configurations of CHB-MLI generate 125 and 243 level output voltage using five Cascaded H-Bridges (CHBs). These DC voltage levels generate staircase output voltage with an equal interval of voltage value between each voltage level. Output voltage waveform is stepped sinusoidal waveform with lower THD. It results in a smoother waveform that is required by the sensitive loads and reduces line losses. The use of an optimum switching technique of PWM is essential for the implementation of the MLIs. According to [18], MLI with a slower switching frequency tends to have lower losses. Phase-Shifted PWM (PSPWM), Space Vector PWM (SVPWM), Sinusoidal PWM (SPWM), and Level-Shifted PWM (LSPWM) have faster switching frequency [19]. Even though THD produced by SVPWM is lesser, its implementation becomes complex for the higher number of levels [19]. Space Vector Control (SVC), Selective Harmonic Elimination (SHE), and Nearest Level Control (NLC) are used as slower switching frequency PWM techniques [20]. But their implementation is not feasible for higher levels [21]. To implement the idea proposed in this research paper, switching sequences are generated for each output voltage level through binary search algorithm and then verified through both the simulation as well as the hardware.
The classification of the remaining portion of the paper is as follows. Section II elaborates the research methodology for the implementation of the proposed solution. Section III explains the simulation through MATLAB Simulink while section IV explains the hardware implementation through STM32F407 VGTX. Section V explains the THD analysis of the output voltage waveform followed by section VI explaining the conclusion.

II. Research Methodology

An H-bridge consists of 4 switches S_1, S_2, S_3 and S_4 as shown in Fig. 1. It is considered that S_1 and S_3 are the switches of one leg while S_2 and S_4 are the switches of other leg. Two switches of the same leg can't conduct at the same time since it will cause the short circuiting. For achieving zero state in a cascaded H-bridge circuit, switches S_1 and S_2 or S_3 and S_4 must be in on condition otherwise it will be considered as a floating H-bridge circuit.

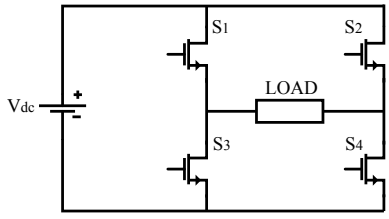


Fig. 1: Circuit diagram of an H-Bridge

Table I depicts different scenario of the output voltage of the H-bridge and respective states of the switches.

Since the proposed configuration generates 125 and 243 levels using five H-bridges, the DC voltages of H-bridges are

TABLE I: Switch States

Switch	$V_0 = V_{dc}$	$V_0 = 0$	$V_0 = -V_{dc}$
S1	1	1	0
S2	0	1	1
S3	0	0	1
S4	1	0	0

in the ratio of 1E, 3E, 9E, 20E and 29E in case of 125-level inverter while 1E, 3E, 9E, 27E and 81E in case of 243-level inverter where E is the constant factor that is used to achieve the standard voltage value either in RMS or peak value. It can also be considered that E is the constant interval between each voltage level. The sum of voltages across all the H-bridges results in output voltage, so the H-bridges are turned ON and OFF for positive, negative and zero voltage in such a way that the sum of voltages across all the switches is equal to the desired output voltage. Switching sequences for all the required output voltage levels for 125 and 243 level inverters are generated using Table I. Fig. 2 shows the circuit diagram of 5 cascaded H-bridges for a single phase. Fig. 3 shows the direction of flow of current and state of different switches for some selected output voltage levels.

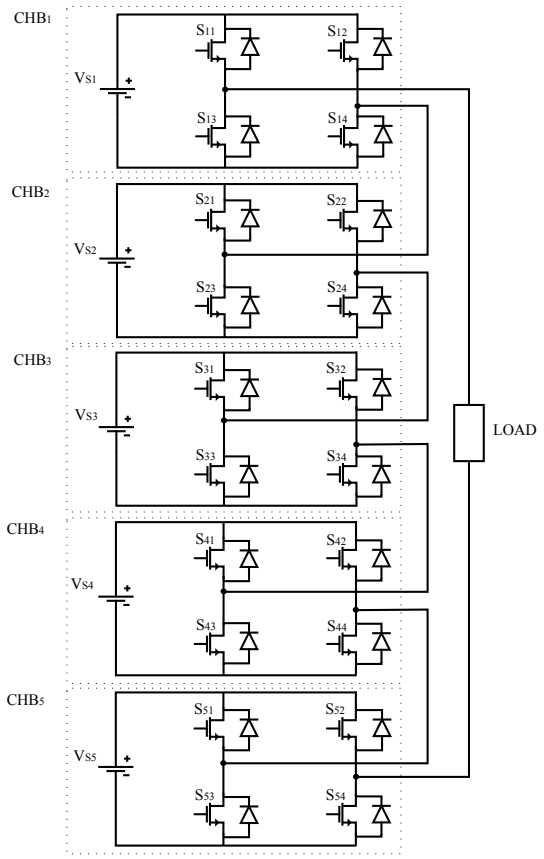
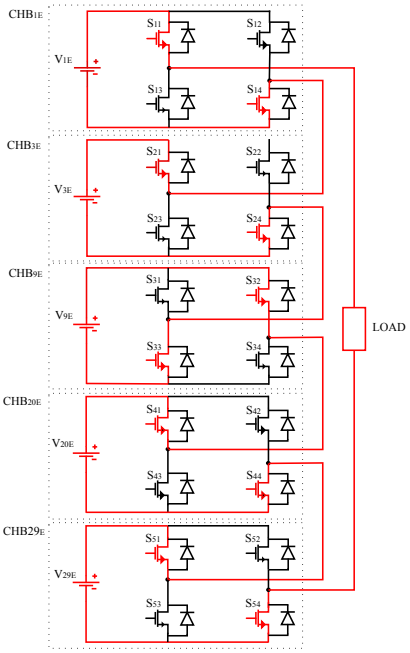


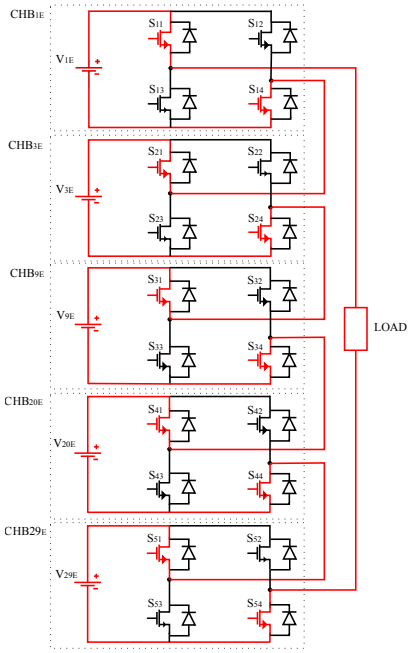
Fig. 2: Circuit diagram of 5 Cascaded H-Bridges

III. Simulation and Results

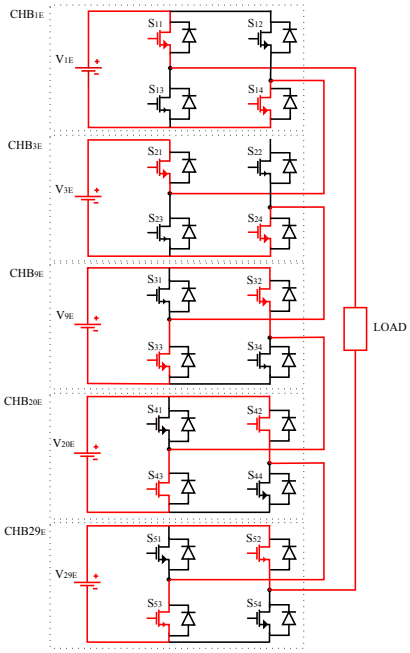
1) Binary Search Algorithm: The switching sequences generate the triangular output voltage waveform. To convert it



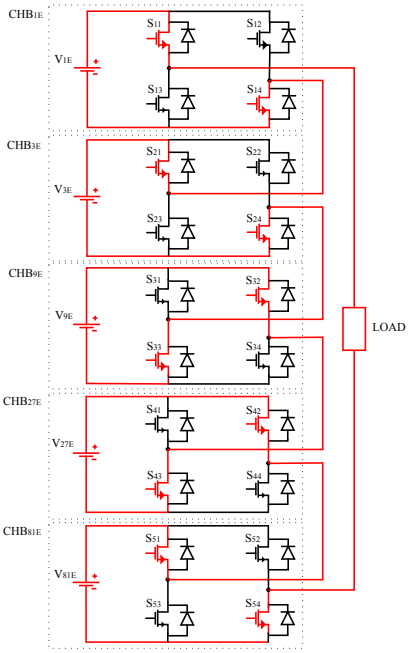
(a) 44E output voltage in 125-level inverter



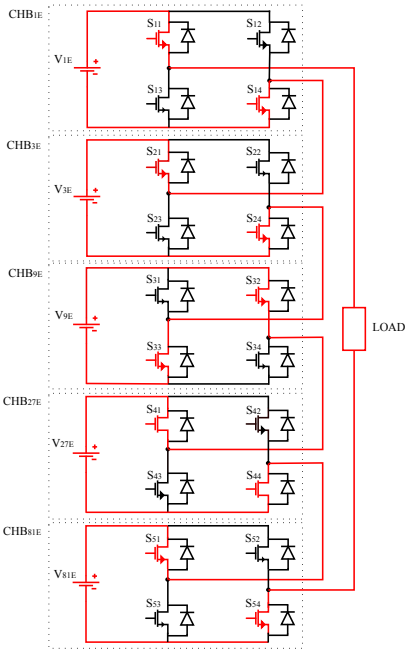
(b) 62E output voltage in 125-level inverter



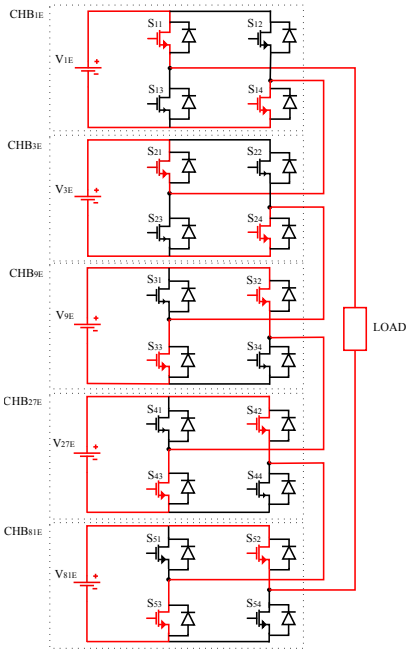
(c) -54E output voltage in 125-level inverter



(d) 49E output voltage in 243-level inverter



(e) 103E output voltage in 243-level inverter



(f) -113E output voltage in 243-level inverter

Fig. 3: Combinatons of H-bridges for required output voltage

to sinusoidal, binary search algorithm is used. Binary search algorithm helps in determining the particular entry in the array. For the implementation of binary search algorithm, switching sequences along with each voltage level are placed in an array S. A sinusoidal waveform is generated as a reference signal to mimic the sensed voltage of grid. Magnitudes of sinusoidal waveform are found from the array of switching sequences and respective switching sequence is then implemented to achieve that voltage level.

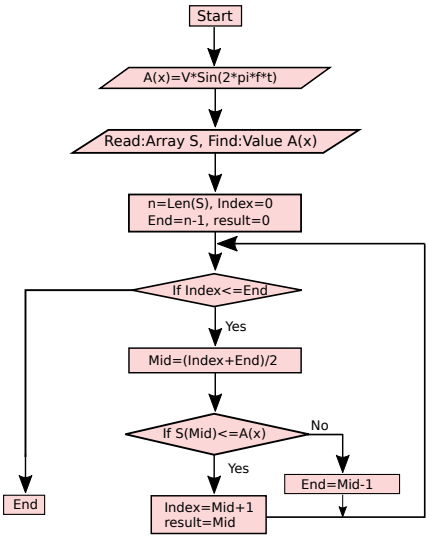


Fig. 4: Binary Search Algorithm

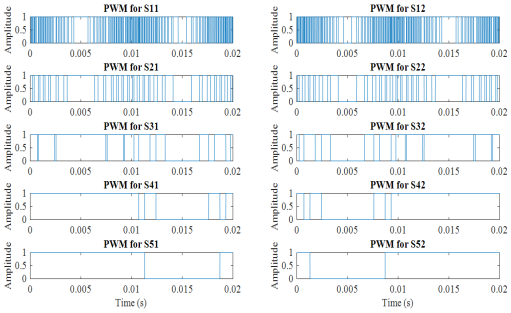


Fig. 5: Designed PWM for 125-level output voltage

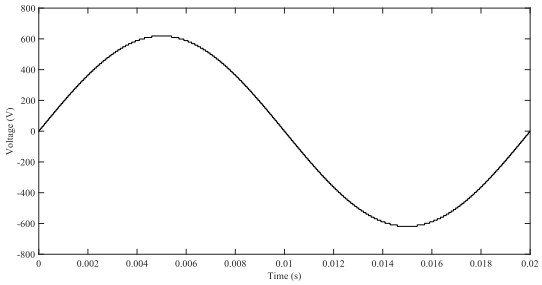


Fig. 6: Single phase 125-level output voltage

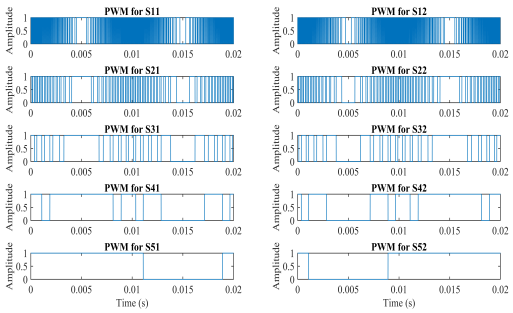


Fig. 7: Designed PWM for 243-level output voltage

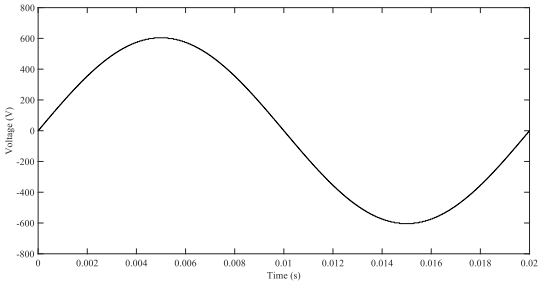


Fig. 8: Single phase 243-level output voltage

IV. Hardware Implementation

Major components used in hardware are:

- MOSFET IRFP450
- Gate Driver TLP250
- STM32F407 Microcontroller

Major parts of the hardware implementation are:

- STM32F407 VGTX Implementation
- Transformer Designing
- Rectifier Circuits

1) STM32F407 Implementation: STM32F407 is used as a microcontroller for the implementation of proposed configuration. STMCubeMX, Keil uVision and STM Studio are used for the implementation through STM.

2) Transformer Designing: Transformers are used for two purposes here.

- To feed the threshold voltage to each switch
- To feed DC Voltage to H-Bridge

For each switch, small transformer of 250/12V are used. While for feeding H-Bridges, a transformer with single primary and five secondaries is designed. This transformer is designed to achieve the required DC Voltage levels of $V_{S1}, V_{S2}, V_{S3}, V_{S4}, and V_{S5}$

3) Rectifier Circuits: Since DC voltage is required for each switch as well as H-Bridge so rectifier or converter circuits are used to convert output of transformer to DC value. Full wave rectifiers are used to achieve constant DC voltage.

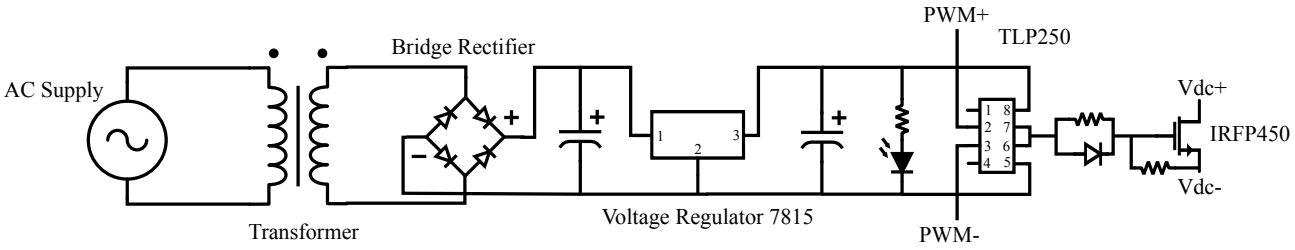


Fig. 9: Circuit Diagram of one switch of H-Bridge

$$V_{dc} = (1.41 * V_{rms}) – 1.4$$

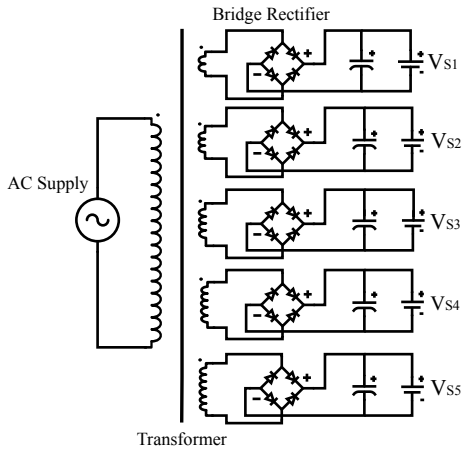


Fig. 10: Rectifier Circuit for each H-Bridge

Fig. 9 shows the circuit diagram of one switch of an H-bridge while Fig. 11 shows the flow chart of the hardware implementation for achieving 125 and 243 level MLIs. Fig. 12 shows the hardware circuit for implementing the proposed asymmetrical configurations. Fig. 14 and Fig. 15 shows the output results of MLIs on CRO.

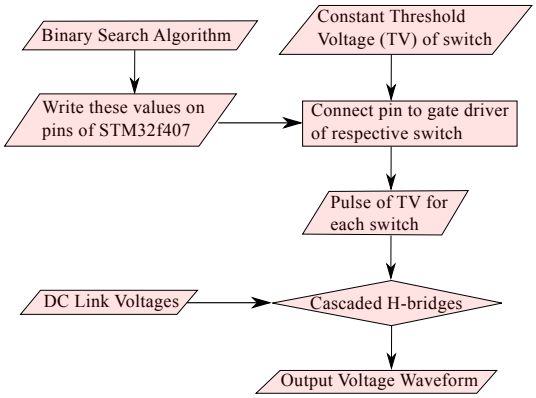


Fig. 11: Hardware Implementation

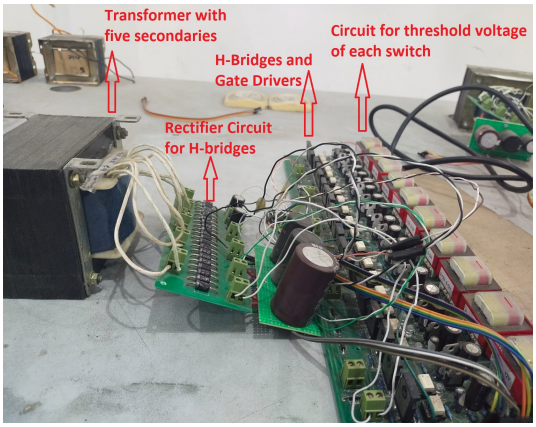


Fig. 12: Circuit for Single Phase 125 and 243 Level Inverter

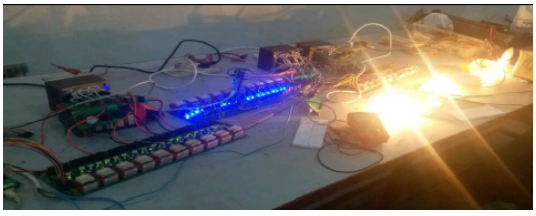


Fig. 13: Load running on 3 Phase 125 Level Inverter

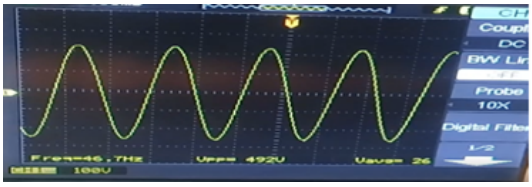


Fig. 14: Output of Single Phase 125 Level Inverter

Fig. 15: Output of Three Phase 125 Level Inverter

V. Total Harmonic Distortion

According to IEEE-519 (standard for THD), THD of the waveform should not exceed 3 percent to be used as a grid-tied inverter. The THD of 125-level and 243-level inverters designed in this research paper have 0.65 and 0.34 percent THD as shown in fig. 16 and 17, so they can easily be used as grid tied inverters.

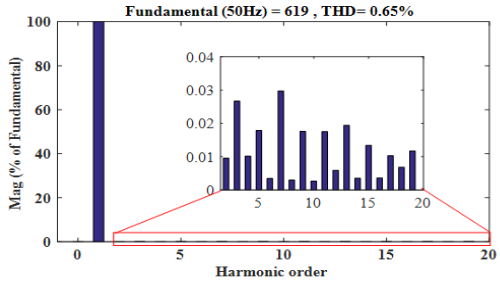


Fig. 16: THD of 125-level output voltage

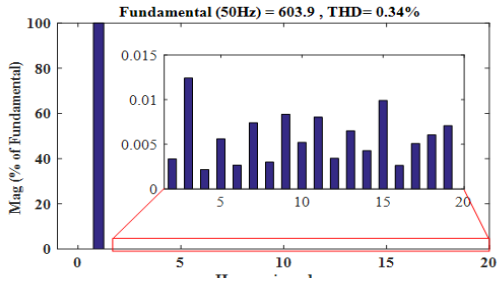


Fig. 17: THD of 243-level output voltage

VI. Conclusion

This paper presents two new asymmetrical configurations for enhancing number of levels and reducing THD to make it feasible to be used as grid tied inverter. Since the THD of both the configurations is within the recommended values by IEEE-519 standard, a closed loop feedback control system can be designed and the reference sinusoidal wave in binary search algorithm can be replaced with grid sensed voltage to be used as a grid tied inverter.

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